ABSTRACT OF THE DISCLOSURE

An electrically writable/erasable nonvolatile semiconductor memory such as an AND-type or NOR-type flash memory having an array structure, in which numerous memory cells are connected in parallel between common bit lines and source lines, is capable of readily detecting a memory cell in depletion failure which occurs in the event of a power supply cutoff during a memory cell threshold voltage shift-down operation by the writing or erasing operation. In operation, at the entry of a certain command or at the time of power-on, all word lines are unselected and bit line selecting switches are turned on to find the presence of a memory cell having a current flow due to depletion failure with sense amplifiers connected to the bit lines. On finding the presence of a failing cell, a voltage of selection level (VSS or negative voltage) is applied to each word line in turn, with remaining word lines being pulled to an unselection voltage level (negative voltage or VSS).